NOTICE OF REVISION (NOR) This revision described below has been authorized for the document listed.	1. DATE (YYMMDD) 93-07-29	Form Approved OMB No. 0704-0188

Public reporting burden for this collection is estimated to average 2 hours per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Department of Defense, Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188), Washington, DC 20503. PLEASE DO NOT RETURN YOUR COMPLETED FORM TO EITHER OF THESE ADDRESSED. RETURN COMPLETED FORM TO THE GOVERNMENT ISSUING CONTRACTING OFFICER FOR THE CONTRACT/ PROCURING ACTIVITY NUMBER LISTED IN ITEM 2 OF THIS FORM.

2. PROCURING ACTIVITY NO.	
3. DODAAC	

4. ORIGINATOR	b. ADDRESS (Street, City, State, Zip Code)	5. CAGE CODE 67268	6. NOR NO. 5962-R207-93
a. TYPED NAME (First, Middle Initial, Last)	Defense Electronics Supply Center 1507 Wilmington Pike Dayton, OH 45444-5270	7. CAGE CODE 67268	8. DOCUMENT NO. **5962-87539**

9. TITLE OF DOCUMENT MICROCIRCUITS, MEMORY, DIGITAL, CMOS UV ERASABLE, PROGRAMMABLE ARRAY LOGIC, MONOLITHIC SILICON	10. REVISION LETTER a. CURRENT G	 b. NEW H	11. ECP NO. 5962-87539ECP-2

12. CONFIGURATION ITEM (OR SYSTEM) TO WHICH ECP APPLIES
ALL

13. DESCRIPTION OF REVISION

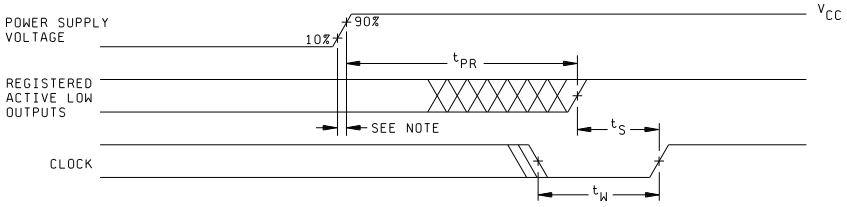
Sheet 1: Revisions ltr column; add "H".
Revisions description column; add "Changes in accordance with NOR 5962-R207-93".
Revisions date column; add "93-07-29".
Revision level block; add "H".
Rev status of sheets; For sheets 6, and 14, add "H".

Sheet 6: Add the following line to the bottom of table I and before the footnotes for table I:

Power up reset time	**t_{PR}**		**9,10,11**	**All**	**1.0** **µs**

Revision level block; delete G and add "H".

Sheet 14: Add the following waveform at the bottom of page, but above the "FIGURE 5. Switching waveforms.", line.



Revision level block; delete G and add "H".

14. THIS SECTION FOR GOVERNMENT USE ONLY

a. (X one)		
	X	(1) Existing document supplemented by the NOR may be used in manufacture.
		(2) Revised document must be received before manufacturer may incorporate this change.
		(3) Custodian of master document shall make above revision and furnish revised document.

b. ACTIVITY AUTHORIZED TO APPROVE CHANGE FOR GOVERNMENT DESC-ECS	c. TYPED NAME (First, Middle Initial, Last) Kenneth S. Rice	
d. TITLE Microelectronics Branch Chief	e. SIGNATURE Michael A. Frye	f. DATE SIGNED (YYMMDD) 93-07-29
15a. ACTIVITY ACCOMPLISHING REVISION DESC-ECS	b. REVISION COMPLETED (Signature) Kenneth S. Rice	c. DATE SIGNED (YYMMDD) 93-07-29

NOTICE OF REVISION (NOR) (See MIL-STD-480 for instructions) This revision described below has been authorized for the document listed.	DATE (YYMMDD) 93-06-17	Form Approved OMB No. 0704-0188

Public reporting burden for this collection is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Information and Regulatory Affairs, Office of Management and Budget, Washington, DC 20503.

1. ORIGINATOR NAME AND ADDRESS	2. CAGE CODE 67268	3. NOR NO. 5962-R187-93
Defense Electronics Supply Center Dayton, Ohio 45444-5277	4. CAGE CODE 67268	5. DOCUMENT NO. 5962-87539
6. TITLE OF DOCUMENT **MICROCIRCUIT, MEMORY, DIGITAL, CMOS UV ERASABLE PROGRAMMABLE ARRAY LOGIC, MONOLITHIC SILICON.**	7. REVISION LETTER (Current) F	(New) G
	8. ECP NO. 5962-87539ECP-1	

9. CONFIGURATION ITEM (OR SYSTEM) TO WHICH ECP APPLIES
ALL

10. DESCRIPTION OF REVISION

Sheet 1: Revisions ltr column; add "G"
Revisions description column; add "Changes in accordance with NOR 5962-R187-93".
Revisions date column; add "93-06-17".
Revision level block; delete "F" and substitute "G".
Rev block above sheet numbers 1, 8, and 15 delete "F" and substitute "G".

Sheet 8: Paragraph 4.3.1d; end of first sentence after the word "herein" add ", or at the manufacturer's option, built-in test circuitry may be used to verify programmability and ac performance without programming the user array."
Revision level block; delete "F" and substitute "G".

Sheet 15: Table II; add "or 2, 8A, 10" in subgroups column for groups C and D end-point electrical parameters.
Revision level block; delete "E" and substitute "G".

11. THIS SECTION FOR GOVERNMENT USE ONLY

CHECK ONE		
[X] EXISTING DOCUMENT SUPPLEMENTED BY THIS NOR MAY BE USED IN MANUFACTURE.	[ ] REVISED DOCUMENT MUST BE RECEIVED BEFORE MANUFACTURER MAY INCORPORATE THIS CHANGE.	[ ] CUSTODIAN OF MASTER DOCUMENT SHALL MAKE ABOVE REVISION AND FURNISH REVISED DOCUMENT TO:

b. ACTIVITY AUTHORIZED TO APPROVE CHANGE FOR GOVERNMENT DESC-ECS	SIGNATURE AND TITLE MICHAEL FRYE BRANCH CHIEF	DATE (YYMMDD) 93-06-17
12. ACTIVITY ACCOMPLISHING REVISION DESC-ECS	REVISION COMPLETED (Signature) RAJESH PITHADIA	DATE (YYMMDD) 93-06-17

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
C	Delete programming waveforms, 4.5.1, 4.5.2, and table III. Changes to 4.5 and 6.6. Editorial changes throughout. Redrawn.	1990 JUN 25	M. Poelking
D	Change C_{IN} and C_{OUT} in table I, IAW NOR 5962-R003-9I.	1991 SEP 20	M. A. Frye
E	Add device type 05; editorial changes throughout. Redrawn.	1993 FEB 02	M. A. Frye
F	Add device type 06; editorial changes throughout. Redrawn.	1993 MAY 04	M. A. Frye

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																				
SHEET																				
REV	E	E																		
SHEET	15	16																		

REV STATUS OF SHEETS	REV	F	F	E	F	F	F	E	F	F	B	B	B	E	B
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Kenneth Rice

CHECKED BY
Ray Monnin

APPROVED BY
M. A. Frye

DRAWING APPROVAL DATE
1987-10-20

REVISION LEVEL
F

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUITS, MEMORY, DIGITAL, CMOS UV ERASABLE, PROGRAMMABLE ARRAY LOGIC, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-87539

SHEET 1 OF 16

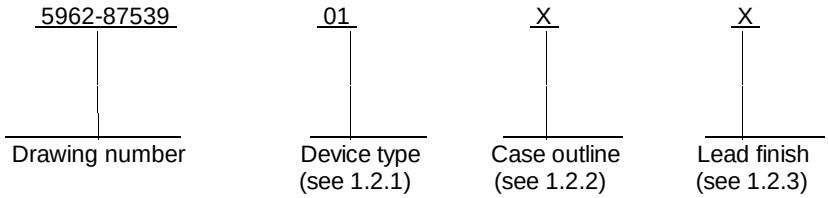
DESC FORM 193
JUL 91

5962-E287-93

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	t_{PD}
01	C22V10	22-input 10-output AND-OR-logic array	25 ns
02	C22V10	22-input 10-output AND-OR-logic array	30 ns
03	C22V10	22-input 10-output AND-OR-logic array	40 ns
04	C22V10	22-input 10-output AND-OR-logic array	20 ns
05	C22V10	22-input 10-output AND-OR-logic array	15 ns
06	C22V10	22-input 10-output AND-OR-logic array	10 ns

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
K	GDFP2-F24, CDFP3-F24	24	Flat package 1/
L	GDIP3-T24, CDIP4-T24	24	Dual-in-line package 1/
3	CQCC1-N28	28	Square chip carrier package 1/
X	GQCC1-J28	28	"J" lead chip carrier package 1/

1.2.3 Lead finish. The lead finish shall be as specified in MIL-M-38510. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 2/

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-2.0 V dc to +7.0 V dc 3/
Output voltage applied range	-0.5 V dc to +7.0 V dc 3/
Output sink current	16 mA
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835
Maximum power dissipation (P_D) 4/	1.2 W
Maximum junction temperature	+175°C
Lead temperature (soldering, 10 seconds maximum)	+260°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc
High level input voltage (V_{IH})	2.0 V dc minimum
Low level input voltage (V_{IL})	0.8 V dc maximum

1/ Lid shall be transparent to permit ultraviolet light erasure.
2/ All voltages referenced to V_{SS}.
3/ Minimum voltage is -0.6 V dc which may undershoot to -2.0 V dc for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} +0.75 V dc which may overshoot to +7.0 V dc for pulses of less than 20 ns.
4/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and bulletin. Unless otherwise specified, the following specification, standards, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standards, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 2.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in screening (see 4.2 herein) or qualification conformance inspection, groups A, B, or C (see 4.3), the devices shall be programmed by the manufacturer prior to test. A minimum of 50 percent of the total number of cells shall be programmed or at least 25 percent of the total number of cells to any altered item drawing.

3.2.3.2 Programmed devices. The truth table for programmed devices shall be as specified by an attached altered item drawing.

3.2.4 Logic diagram(s). The logic diagram(s) shall be as specified on figure 3.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ V_{SS} = 0 V -55°C ≤ T_C ≤ +125°C 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	I_O = -2.0 mA	1, 2, 3	All	2.4		V
Low level output voltage	V_{OL}	I_O = 12.0 mA	1, 2, 3	All		0.5	V
High impedance output leakage current 2/	I_{OZ}	V_O = GND and V_O = 5.5 V V_{CC} = 5.5 V	1, 2, 3	All	-40	40	µA
High level input current	I_{IH}	V_{IH} = 5.5 V	1, 2, 3	All		10	µA
Low level input current	I_{IL}	V_{IL} = GND	1, 2, 3	All		-10	µA
Supply current	I_{CC}	V_{CC} = 5.5 V	1, 2, 3	01-05		100	mA
				06		160	
Output short circuit current 3/ 4/	I_{OS}	V_{CC} = 5.5 V V_O = 0.5 V	1, 2, 3	01-05	-30	-90	mA
				06	-30	-120	
Input capacitance	C_{IN} 4/ 5/	V_I = 0 V, V_{CC} = 5.0 V T_A = +25°C, f = 1 MHz See 4.3.1c	4	All		10	pF
Output capacitance	C_{OUT} 4/ 5/	V_O = 0 V, V_{CC} = 5.0 V T_A = +25°C, f = 1 MHz See 4.3.1c	4	All		10	pF
Functional testing		See 4.3.1e	7, 8	All			
Input or feedback to non-registered output	t_{PD}	V_{CC} = 4.5 V, C_L = 50 pF See figure 4, circuit B and figure 5	9, 10, 11	01		25	ns
				02		30	
				03		40	
				04		20	
				05		15	
				06		10	
Clock to output	t_{CO}		9, 10, 11	01,04		15	ns
				02		20	
				03		25	
				05		10	
				06		8	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ V_{SS} = 0 V -55°C ≤ T_C ≤ +125°C 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input to output enable	t_{EA}	V_{CC} = 4.5 V, C_L = 5 pF See figure 4, circuit A and figure 5	9, 10, 11	01		25	ns
				02		30	
				03		40	
				04		20	
				05		15	
				06		10	
Input to output disable	t_{ER}		9, 10, 11	01		25	ns
				02		30	
				03		40	
				04		20	
				05		15	
				06		10	
Clock period	t_P	V_{CC} = 4.5 V, C_L = 50 pF See figure 4, circuit B, and figure 5	9, 10, 11	01	33		ns
				02	40		
				03	55		
				04	32		
				05	20		
				06	7		
Clock pulse width 4/ 6/	t_W		9, 10, 11	01,04	15		ns
				02	20		
				03	27		
				05	6		
				06	3.5		
Setup time 4/ 6/	t_S		9, 10, 11	01	18		ns
				02	20		
				03	30		
				04	17		
				05	10		
				06	5		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ V_{SS} = 0 V, -55°C ≤ T_C ≤ +125°C, 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Hold time 4/ 6/	t_H		9, 10, 11	All	0		ns
Maximum clock frequency 4/ 6/ $1/(t_{CO} + t_S)$	f_{MAX}	V_{CC} = 4.5 V, C_L = 50 pF See figure 4, circuit B, and figure 5	9, 10, 11	01	30		MHz
				02	25		
				03	18		
				04	31		
				05	50		
				06	77		
Asynchronous reset pulse width	t_{AW}	V_{CC} = 4.5 V, C_L = 50 pF See figure 4, circuit B and figure 5	9, 10, 11	01	25		ns
				02	30		
				03	40		
				04	20		
				05	15		
				06	7		
Asynchronous reset recovery time	t_{AR}		9, 10, 11	01	25		ns
				02	30		
				03	40		
				04	20		
				05	15		
				06	8		
Asynchronous reset to registered output reset	t_{AP}		9, 10, 11	01,04		25	ns
				02		30	
				03		40	
				05		20	
				06		14	

1/ All voltages are referenced to ground.
2/ I/O terminal leakage is the worst case of I_{IX} or I_{OZ}.
3/ Only one output shorted at a time.
4/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
5/ All pins not being tested are to be open.
6/ Test applies only to registered outputs.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations; two processing options are provided for selection in the contract.

3.10.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 3.2.3.1 and table IIA. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.10.2 Manufacturer programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

3.11 Processing EPLDS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.11.1 Erasure of EPLDS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4.

3.11.2 Programmability of EPLDS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5.

3.11.3 Verification of erasure or programmed EPLD's. When specified, devices shall be verified as either programmed (see 4.5 herein) to the specified pattern or erased (see 4.4 herein). As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps:

Margin test method A. * Steps 1 through 3 may be performed at wafer level.

*(1) Program greater than 95 percent of the bit locations, including the slowest programming cell. The remaining cells shall provide a worst case speed pattern.

*(2) Bake, unbiased, for 72 hours at +140°C or for 48 hours at +150°C or for 8 hours at +200°C, or 2 hours at +300°C for unassembled devices only.

*(3) Perform margin test using V_m = +5.7 V minimum at +25°C using loose timing (i.e., t_{ACC} = 1 µs).

(4) Perform dynamic burn-in (see 4.2a).

(5) Perform margin test using V_m = +5.7 V at +25°C.

(6) Perform electrical tests (see 4.2).

(7) Erase (see 3.10.1). Devices may be submitted for groups A, B, C, and D testing.

(8) Verify erasure (see 3.10.3).

The maximum storage temperature shall not exceed +200°C for packaged devices or +300°C for unassembled devices.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured for the initial characterization and after any process or design changes which affect capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

d. All devices submitted for testing shall be programmed in accordance with 3.2.3.1 or 3.2.3.2 herein. After completion of all testing, the devices shall be erased and verified except devices submitted to groups C and D testing.

e. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

c. All devices submitted for testing shall be programmed in accordance with 3.2.3.1 or 3.2.3.2 herein. After completion of all testing, the devices shall be erased and verified.

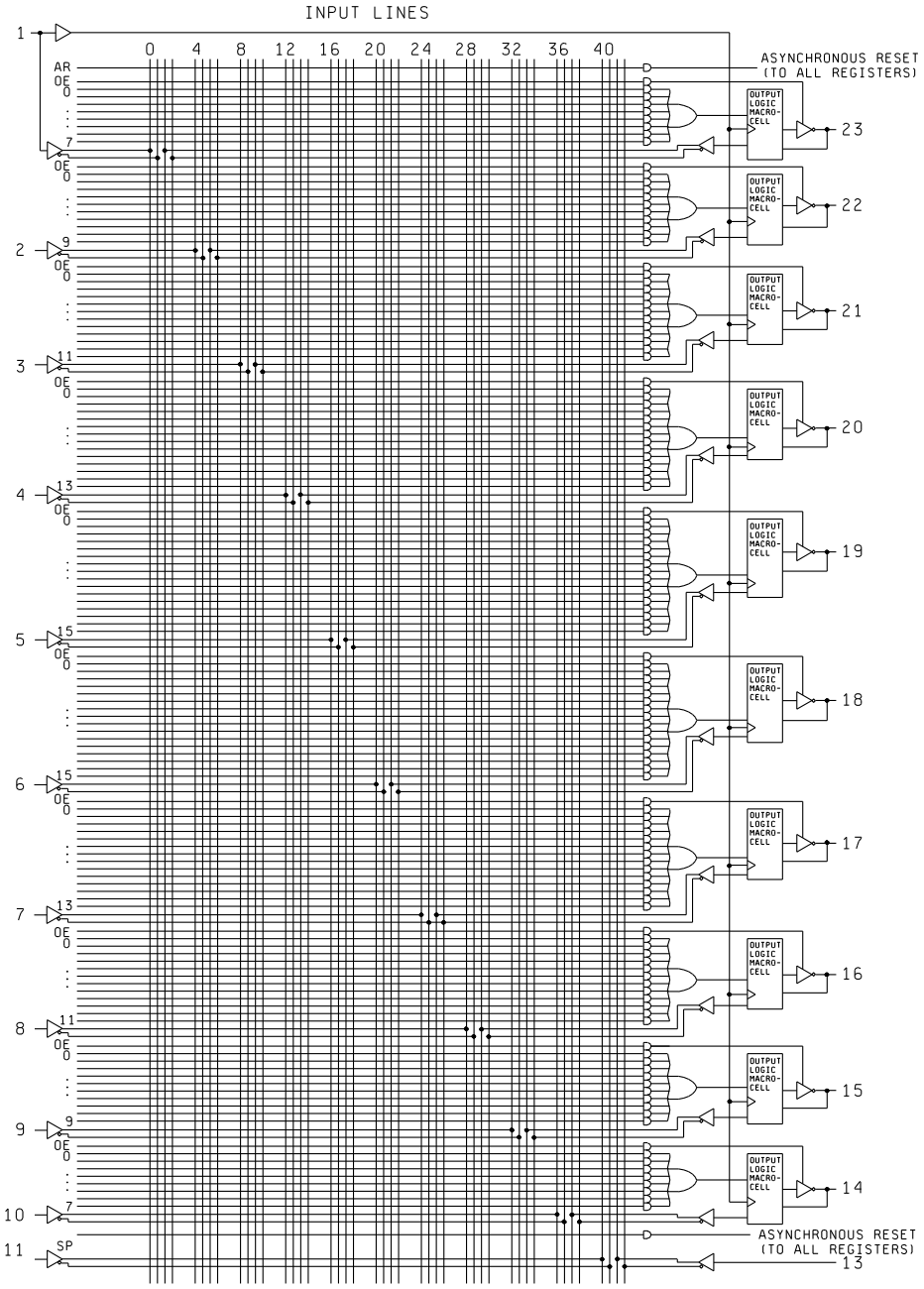
Device types	01, 02, 03, 04, 05, and 06	
Case outlines	K, L	3, X
Terminal number	Terminal symbol	
1	CP/I	NC
2	I	CP/I
3	I	I
4	I	I
5	I	I
6	I	I
7	I	I
8	I	NC
9	I	I
10	I	I
11	I	I
12	GND	I
13	I	I
14	I/O	GND
15	I/O	NC
16	I/O	I
17	I/O	I/O
18	I/O	I/O
19	I/O	I/O
20	I/O	I/O
21	I/O	I/O
22	I/O	NC
23	I/O	I/O
24	V_{CC}	I/O
25	---	I/O
26	---	I/O
27	---	I/O
28	---	V_{CC}

FIGURE 1. Terminal connections.

Truth table																					
Input pins												Output pins									
CP/I	I	I	I	I	I	I	I	I	I	I	I	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
X	X	X	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

NOTES:
1. Z = Three-state
2. X = Don't care

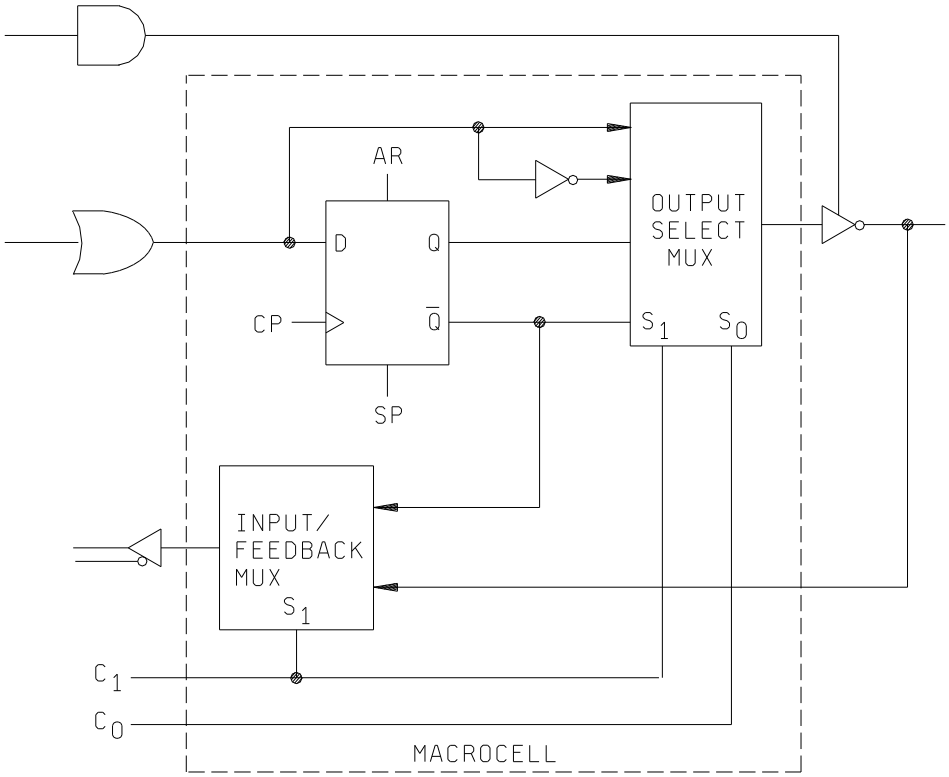
FIGURE 2. Truth table (unprogrammed).



NOTE: PIN numbers apply to cases K and L only.

FIGURE 3. Logic diagram (unprogrammed).

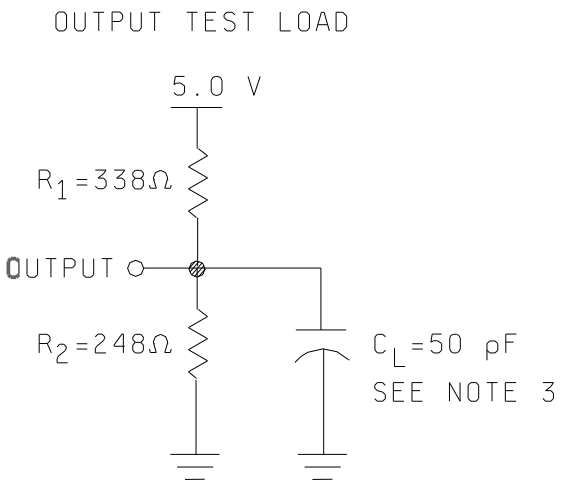
Output logic macrocell



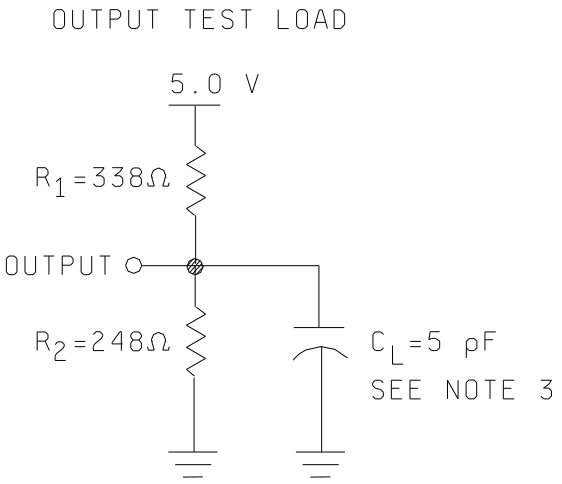
C_1	C_0	Output configuration
0	0	Registered/active low
0	1	Registered/active high
1	0	Combinatorial/active low
1	1	Combinatorial/active high

0 = Logical zero
1 = Logical one

FIGURE 3. Logic diagram (unprogrammed) - Continued.



Circuit B or equivalent



Circuit A or equivalent (t_{EA} and t_{ER})

NOTES:
1. AC testing. Inputs pulse levels are 0 to 3.0 V with transition times of 5 ns or less. Timing reference levels are 1.5 V unless otherwise specified.
2. t_{EA} transition is measured ±500 mV from steady-state voltage.
3. Including jig and scope (minimum value).

FIGURE 4. Output test circuits.

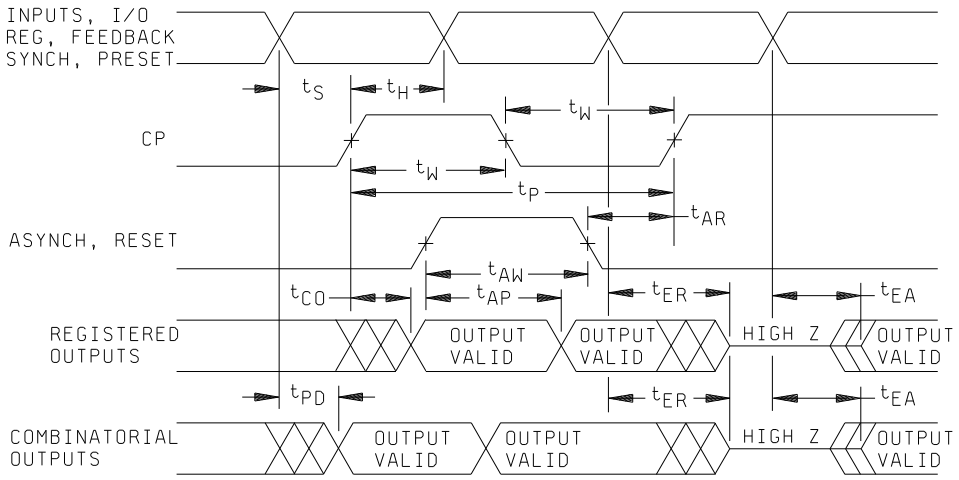


FIGURE 5. Switching waveforms.

TABLE II. Electrical test requirements. 1/ 2/ 3/ 4/

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*,2,3,7*,8,9
Group A test requirements (method 5005)	1,2,3,4**,7, 8,9,10,11
Groups C and D end-point electrical parameters (method 5005)	2,3,7,8

1/ * indicates PDA applies to subgroups 1 and 7.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ ** see 4.3.1c.
4/ Subgroups 7 and 8 functional tests shall also verify no cells are programmed for unprogrammed devices or the altered item drawing pattern exists for programmed devices.

4.4 Erasing procedure. The recommended erasure procedure for the device is exposure to shortwave ultraviolet light which has a wavelength of 2537 angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 25 Ws/cm^2. The erasure time with this dosage is approximately 35 minutes using a ultraviolet lamp with a 12,000 uW/cm^2 power rating. The device should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is 7258 Ws/cm^2 (1 week at 12,000 uW/cm^2). Exposure of the device to high intensity UV light for long periods may cause permanent damage.

4.5 Programming procedure. The programming procedure shall be as specified by the device manufacturer and shall be made available upon request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for original equipment manufacturer application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 93-05-04

Approved sources of supply for SMD 5962-87539 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-8753901KX	1FN41 65786	AT22V10-25YM/883 PALC22V10-25TMB
5962-8753901LX	1FN41 65786	AT22V10-25DM/883 PALC22V10-25WMB
5962-87539013X	1FN41 65786	AT22V10-25LM/883 PALC22V10-25QMB
5962-8753902KX	1FN41 65786	AT22V10-30YM/883 PALC22V10-30TMB
5962-8753902LX	1FN41 50364 65786	AT22V10-30DM/883 PALC22V10H-30MQS/883B PALC22V10-30WMB
5962-87539023X	1FN41 65786	AT22V10-30LM/883 PALC22V10-30QMB
5962-8753903KX	1FN41 65786	AT22V10-40YM/883 PALC22V10-40TMB
5962-8753903LX	1FN41 50364 65786	AT22V10-40DM/883 PALC22V10H-40MQS/883B PALC22V10-40WMB
5962-87539033X	1FN41 65786	AT22V10-40LM/883 PALC22V10-40QMB
5962-8753904KX	1FN41 65786	AT22V10-20YM/883 PALC22V10B-20TMB
5962-8753904LX	1FN41 65786	AT22V10-20DM/883 PALC22V10B-20WMB
5962-87539043X	1FN41 65786	AT22V10-20LM/883 PALC22V10B-20QMB
5962-8753905LX	1FN41	AT22V10-15DM/883
5962-87539053X	1FN41	AT22V10-15LM/883
5962-8753905KX	1FN41	AT22V10-15YM/883
5962-8753906LX	1FN41	AT22V10B-10DM/883
5962-87539063X	1FN41	AT22V10B-10LM/883
5962-8753906XX	1FN41	AT22V10B-10KM/883

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address	Margin test method
1FN41	ATMEL Corporation 2125 O'Nel Drive San Jose, CA 95131	A
50364	MMI/AMD 2175 Mission College Boulevard Santa Clara, CA 95054-1592 Point of contact: 901 Thompson Place P.O. Box 3453 Sunnyvale, CA 94088	A
65786	Cypress Semiconductor Corporation 3901 North First Street San Jose, CA 95134	A

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.